ABSTRACT

A digital signal processing chip having a multiple processor cores with corresponding processor subsystems, a shared component, and a clock tree, is disclosed herein. A clock tree distributes clock signals to the processor cores and the shared component. The clock tree can be configured to disable one or more of the processor cores and the shared component by blocking the corresponding clock signal. This may advantageously conserve power. However, the clock tree is configured to preserve the clock signal to the shared component as long as at least one of the processor cores has not disabled the shared component. That is, to block the clock signal to the shared component, each of the processor cores must disable the shared component. The shared component may, for example, be a shared program memory or an arbiter for an external input/output port. The clock tree may include a register and a series of clock gates. Each of the clock gates blocks the clock signal when a gate signal is de-asserted. The gate signals are generated from enablement bits in the register. The clock signal for the shared component is gated by a clock gate that blocks the clock signal only if each of the processor cores have disabled their enablement bit for the shared component.